WHAT IS CLAIMED IS:

1. An adjustable harmonic distortion detector comprising:

a clock signal source;

means for detecting a first period of evaluation;

means for detecting a second period of evaluation;

a first block for memorizing a number equal to the clock pulses present in the first period of evaluation;

a multiplier block for performing a multiplication between the number stored in the first block and a multiplicative factor during the second period of evaluation; and

a second block for memorizing the outcome of the multiplication, the second block adapted to generate an output signal when the outcome in the second block is equal to zero.

2. The distortion detector according to the claim 1, wherein the multiplicative factor is a predetermined fixed number.

3. The distortion detector according to the claim 1, wherein the multiplicative factor is function of the number of clock signal pulses stored in the first block.

4. The distortion detector according to the claim 1, wherein the multiplicative factor is deduced from the correlation between the ratio of the second and first period of evaluation and the total distortion value according to a diagram.

5. The distortion detector according to the claim 1,

wherein the first block receives in input the clock signal, the first evaluation period,

the multiplier block receives at input the cloak signal, the multiplicative factor, and the output signal of the first block, and

the second block receives at input the clock signal, the output signal of the multiplier block, the second evaluation period, and produces an output signal during the simultaneous combination of the clock signal and the second evaluation period.

6. The distortion detector according to the claim 1,

wherein the first block receives at input the clock signal, the first evaluation period,

the multiplier block receives at input the clock signal, the second evaluation period, and a signal generated by a fourth block adapted to realize a correspondence function between the number of clock pulses counted in the measure period of the first block and the diagram, and

the second block receives at input the clock signal, the output signal of the multiplier block, the second evaluation period, and it produces an output signal during the second evaluation period.

7. The distortion detector according to claim 1, wherein the first evaluation period provides the length from the crossing of the abscissa axis to the start of the distortion step of the output signals.

8. The distortion detector according to claim 7, wherein the second evaluation period provides the length from the start of the distortion step to the end of the same of the output signals.

9. The distortion detector according to claim 1, wherein the first block and the third block are up counters.

10. The distortion detector according to claim 9, wherein the second block is a down counter.

11. The distortion detector according to claim 10, wherein the fourth block makes the correspondence function between the number of clock pulses counted in the first evaluation period and stored in the first block and the diagram.

12. An adjustable harmonic distortion detector comprising:

a clock signal source;

frequency multiplier/divider means for generating a modified clock signal;

means for detecting a first period of evaluation;

means for detecting a second period of evaluation;

a first block for memorizing a number equal to the clock pulses present in the first period of evaluation;

a third block for counting the clock pulses present in the modified clock signal; and

a comparator for comparing the number stored in the first block with the number stored in the third block, the comparator adapted to generate an output signal when the number in the first block and the number in the third block are equal to zero.

13. The distortion detector according to the claim 12, wherein the frequency multiplier/divider means performs a multiplication/division for a predetermined fixed number.

14. The distortion detector according to the claim 12, wherein the frequency multiplier/divider means performs a multiplication/division for a number function of the value stored in the first block.

15. The distortion detector according to the claim 12,

wherein the first block receives at input the clock signal, the first evaluation period,

the frequency multiplier/divider means receives at input the clock signal,

the third block receives at input the output of the frequency multiplier/divider means, the second evaluation period, and

the comparator receives at input the output signal of the first block, the output signal of the third block and the second evaluation period, and it produces an output signal during the second evaluation period.

16. The distortion detector according to the claim 12,

wherein the first block receives at input the clock signal, the first evaluation period,

the frequency multiplier/divider means receives at input the clock signal, the first evaluation period, and an output signal of a fifth block,

the third block receives at input the output of the frequency multiplier/divider means, the second evaluation period, and

the comparator receives in input the output signal of the first block, the output signal of the third block and the second evaluation period, and it produces an output signal during the second evaluation period.

17. The distortion detector according to claim 12, wherein the first evaluation period provides the length from the crossing of the abscissa axis to the start of the distortion step of the output signals.

18. The distortion detector according to claim 17, wherein the second evaluation period provides the length from the start of the distortion step to the end of the same of the output signals.

19. The distortion detector according to claim 12, wherein the first block and the third block are up counters.

20. The distortion detector according to claim 19, wherein the second block is a down counter.

21. The distortion detector according to claim 20, wherein the fourth block makes the correspondence function between the number of clock pulses counted in the first evaluation period and stored in the first block and the diagram.

22. A method for detecting harmonic distortion, said method comprising the steps of:

computing the length of a first period of evaluation;

computing the length of a second period of evaluation;

receiving at input a predetermined value of total harmonic distortion; and

generating an output signal showing the reaching of the value of the prefixed distortion.

23. A method for detecting harmonic distortion, said method comprising the steps of:

counting a number of clock signal pulses in a first period of evaluation;

inserting the number in a first block;

inserting a multiplicative factor in a second block;

multiplying the value stored in the first block with the value stored in the second block during a second period of evaluation;

decreasing the outcome of the multiplying step during the second period of evaluation;

generating a signal in the case that the outcome of the deceasing step is zero.

24. The method according to the claim 23, wherein the multiplicative factor is a predetermined fixed number.

25. The method according to the claim 23, wherein the multiplicative factor is a value in function of the pulse number stored in the first block.

26. A method for detecting harmonic distortion, said method comprising the steps of:

a) counting a number of clock signal pulses in a first period of evaluation;

b) inserting the number in a first block;

c) modifying the clock signal in a modified clock signal;

d) counting a number of modified clock signal pulses present in a second period of evaluation;

e) inserting the outcome of the step of counting a number of modified clock signal pulses in a third block;

f) comparing the outcomes of the step of inserting the number and the step of inserting the outcome during second period of evaluation;

g) generating an output signal in the case the outcome of the comparing step is equal to zero.

27. The method according to the claim 26, wherein the modified clock signal is deduced by multiplication/division for a predetermined fixed number.

28. The method according to the claim 26, wherein the modified clock signal is deduced by multiplication/division for a number which is a function of the value present in the first block.